



GPON OLT Optical Transceiver SFP Module

DPW-G-M-SFPGPL-24

Features

- Integrated Single fiber
 bi-directional optical subassembly
- 1310nm Burst-mode APD/TIA receiver and 1490nm Continuous DFB laser Transmitter (with WDM)
- SFP metallic package
- 0 to 70°C operating ambient temperature
- Single SC receptacle optical interface compliant

- Hot-pluggable
- +3.3V single power supply
- Low power consumption
- Fast settling time with immunity to long streams of CID
- Guard time squelched function
- Digitalized burst mode optical power monitoring
- LVPECL compatible data input and output interface
- LVTTL receiver reset control



- LVTTL receiver
 burst-power-detect indication
- Class 1 Laser eye safety standard
- Excellent EMI and EMC

characteristics

- ESD protection function
- RoHs compliant

Application

• Optical transceiver for Gigabit-capable Passive Optical Networks (GPON) Class B+ OLT side

Standard

- ITU-T G.984.2 Class B+
- Small Form-factor Pluggable (SFP) Transceiver Multisource Agreement July 5, 2000

Description

The GPON OLT Transceiver is designed for Gigabit-capable Passive Optical Network (GPON) transmission. The module incorporates 1490nm DFB continuous-mode transmitter and 1310nm burst-mode APD receiver.

The transmitter section uses a high efficiency 1490nm DFB laser and an integrated laser driver which is designed to be class-1 eye safety under any single fault. The laser driver includes APC and temperature compensation functions, which are used for keeping the launch optical power and extinction ratio constant over temperature and aging.

The receiver section uses an integrated APD detector and burst mode preamplifier mounted together. To provide fast settling time with immunity to long streams of Consecutive Identical Digits(CID), the receiver requires a reset signal provided by the media access controller(MAC). The receiver has fast SD function, the rising time is about 5ns, when reset signal arrived, the SD signal will be turned to low, and the noise in the guard time will be squelched.

The receiver includes digitalized burst mode optical power monitoring function, which converses any of a received ONU optical power directly in digital, with a Trigger input from system. When rising edge of Trigger detected, the DDM processor starts a burst optical power conversion, the digital result is available via DDM interface after Burst Optical Power Conversion Time. Trigger pulse width should be more than Burst Optical Power Conversion Holding Time.

An integrated WDM coupler can distinguish 1310nm input light from 1490nm output light.

The metallic package guarantees excellent EMI and EMC characteristics, which totally comply with international relevant standards.

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Operating Temperature Range	T _c	°C	0	70
Storage Temperature Range	Ts	°C	-40	85



Relative Humidity	RH	%	5	95
Power Supply Voltage	V _{cc}	V	0	4.6
Pin Input Voltage		V	GND	Vcc
Receiver Damage Threshold		dBm	+4	_

Recommended operating conditions

Parameter	Symbol	Unit	Min	Тур	Max
Operating Voltage	V _{cc}	V	3.135	3.3	3.465
Operating Temperature Range	T _{op}	°C	0	-	70
Operating Data Rate(TX side)		Mbps	_	2488.32	-
Operating Data Rate(RX side)		Mbps	-	1244.16	-

Specifications (0°C<Top<70°C and 3.135V<Vcc<3.465V)

Parameter	Symbol	Unit	Min	Тур	Max	Test condition	
Electri	cal Chara	cteristi	cs				
Operating Voltage	V _{op}	V	3.135	3.3	3.465		
Supply Current	I _{cc}	Ма	200	_	400		
LVPECL Single Ended Data Input Swing		Μv	100	_	1200	Note1	
LVPECL Single Ended Data Output Swing		Μv	640	-	880	Note10	
Differential Data input impedance		Ω	-	100	_	Note1	
Signal Level(LVTTL H)		V	2.4	-	Vcc		
Signal Level(LVTTL L)		V	0	-	0.8		
Optical Transmitter Characteristics							
Data Rate		Mbps	-	2488.32	-		
Center Wavelength Range	λ_{c}	Nm	1480	1490	1500	DFB-LD	
Spectral Width(@-20Db)	$\Delta\lambda$	Nm	-	-	1		
Side Mode Suppression Ratio	SMSR	Db	30	_	-		
Launch Optical Power	Po	dBm	+1.5	—	+5	Note2	
Off level light		dBm		-	-39	Note3	
Extinction Ratio	EX	Db	9.0	-	-	Note4	
Total Jitter	J_{total}	UI	-	-	0.1		
Rise/Fall time(20~80%)	Tr/Tf	Ps	-	—	150	Note5	
RIN ₁₅ OMA		Db/Hz	-	-	-115		
Optical Return Loss Tolerance		Db	-	-	15		
Maximum reflectance		Db	-	_	-12	λ=1.49μm	
Eye Diagram	Cor	mpliant	with ITL	J-T G.984.	2	Note4 Note6	

Note1:AC coupled internal(see the recommended circuit below).

Note2:Coupled into 9/125 SMF

Note3:Measured without data input

Note4: Measured with PRBS 2²³-1 test pattern @2.488Gbps



Note5:Measured with the Bessel-Thompson filter OFF **Note6:**Mask of diagram as below



	1244.16 Mbit/s	2488.32 Mbit/s
x1/x4	0.28/0.72	
x2/x3	0.40/0.60	
x3 – x2		0.2
y1/y2	0.20/0.80	0.25/0.75

Optical Receiver Characteristics							
Data Rate			Mbps	-	1244.16) —	
Receiver Sensitivity		S	dBm	_	_	-28	Note7
Overload Input Optical Power P _{in}		dBm	-8	-	-	Note7	
Center Wavelength Range λ_c		nm	1260	1310	1360		
Receiver Settling Time		T _{settling}	ns	_	-	35	Note8 Figure1
Reset to Data Time		T_{rd}	ns	15	-	_	Note9 Figure1
Reset Pulse Width		T _{reset}	ns	12.8	16	_	Figure1
Guard Time T _{gu}		T _{guard}	ns	25.2	-	_	Note11 Figure1
Receiver reflectance			Db	_	-	-12	λ=1.31μm
Signal Datast (I)(TTL)	Optical Dessert		dBm	-45	-	_	
	Optical Assert		иып	_	-	-30	
Signal Detect Hysteresis	6		Db	0.5	-	6	
Signal Detect response time		Ns		5		Note12 Figure1	
Measurement Accuracy of received burst							
optical power, range from -10dBm to		dB	-2		+2	Note13	
-30dBm							
Burst optical power conv	version settling time	BOPCS	ns	100			Figure 2



	Time				
Burst optical power conversion holding time	Holding Time	ns	400		Figure 2
					result can be read out since
Burst optical power conversion time		us		500	rising edge of the trigger
					pulse

Note7: Measured with PRBS 2^{23} -1 test pattern @1.244Gbps with Tx on, ER=10dB,BER<=10E-10.

Note8:Time from the arrival of data to the output data settling to within 15% of final amplitude and duty-cycle. It is shown in the Figure 1.

Note9: Time from a falling edge on reset signal input to the start of preamble at the data input of the receiver. **Note10:** DC coupled internal. Need LVPECL terminal on the host board.

Note11: Time from end of previous data burst to beginning of next data burst.

Note12: The rising time of SD signal is about 5ns, when RESET signal arrived SD level will turn to low in 5ns. **Note13:** Measured with PRBS23 Burst data pattern @1.244Gbps.



Figure1 Time parameter definition in GPON system







Memory Map

2 wire address 1010000X (A0)

2 wire address 1010001X(A2)





EEPROM Serial ID Memory Contents

Accessing Serial ID Memory uses the 2 wire address 1010000X (A0). Memory Contents of Serial ID are shown in Table below.

Table 1	Serial II	D Memory Contents		
Data Address	Size (Bytes)	Name of Field	Contents(Hex)	Description
			BASE ID FIELDS	
0	1	Identifier	03	SFP
1	1	Ext. Identifier	04	SFP function is defined by serial ID only
2	1	Connector	01	Connector
3-10	8	Transceiver	00 00 00 80 00 00 00 00	
11	1	Encoding	03	NRZ
12	1	BR, Nominal	19	2488.32Mbps
13	1	Reserved	00	
14	1	Length (9µm) km	14	
15	1	Length (9µm) 100m	C8	
16	1	Length (50µm) 10m	00	- Transceiver transmit distance 20km
17	1	Length(62.5µm)10m	00	_
18	1	Length (Copper)	00	Not compliant
19	1	Reserved	00	
20-35	16	Vendor name	57 54 44 20 20 20 20 20 20	"WTD"(ASCII)
36	1	Posorvod	00	
27 20	3	Vender OIII	00 00 00	
37-37	5	Vendor Obr	52 54 58 4D 31 36 37 2D	"DTYM167 500"
40-55	16	Vendor PN	35 32 32 20 20 20 20 20 20	Transcoiver part number
56 50	Λ	Vendor rov	20 20 20 20 20 20 20	
60-61	2	Wavelength	05 D2	1490pm TX wavelength
62	1	Reserved	00	
63	1		Check Sum (Variable)	Check code for Base ID Fields
	•		EXTENDED ID FIELDS	
64-65	2	Options	00 1C	TX_DISABLE, TX_FAULT and Burst Power Detect (SD) implemented.
66	1	BR, max	00	
67	1	BR, min	00	
(0.00	4.4		42 30 30 39 38 32 32 20	Serial Number of transceiver
68-83	16	vendor SN	20 20 20 20 20 20 20 20 20	(ASCII). For example "B009822".
84-91	8	Date code	30 32 31 30 30 35 20 20	Manufactory date code. For example "021005".
92	1	Diagnostic	60	DDM implemented, Internal



		Monitoring Type		calibration	
93	1	Enhanced Options	80	Alarm/warning flags implemented.	
04	1	SFF-8472	02	Pov 9.4 of SEE 8472	
94 1	compliance	02	Nev 7.4 01 311-0472		
95	1	CC_EXT	Check Sum (Variable)	Check sum for Extended ID Field.	
VENDOR SPECIFIC ID FIELDS					
96-127	32	Vendor Specific	Read only	Depends on customer information	
128-255	128	Reserved	Read only	Filled by zero	

Diagnostic Monitor Functions

Diagnostic Monitor Functions interface uses the 2 wire address 1010001X (A2). Memory contents of Diagnostic Monitor Functions are shown in Table below.

Data	Field Size	Namo	Contonts and Description
Address	(bytes)	Name	contents and Description
		Alarm and Warnin	ng Thresholds
00-01	2	Temperature High Alarm	Set to 80 °C
02-03	2	Temperature Low Alarm	Set to -13 °C
04-05	2	Temperature High Warning	Set to 75 °C
06-07	2	Temperature Low Warning	Set to -8 °C
08-09	2	Vcc High Alarm	Set to 3.6 V
10-11	2	Vcc Low Alarm	Set to 3.0 V
12-13	2	Vcc High Warning	Set to 3.5 V
14-15	2	Vcc Low Warning	Set to 3.1 V
16-17	2	Bias High Alarm	90mA
18-19	2	Bias Low Alarm	OmA
20-21	2	Bias High Warning	70mA
22-23	2	Bias Low Warning	OmA
24-25	2	TX Power High Alarm	+5.5dBm
26-27	2	TX Power Low Alarm	+0.5dBm
28-29	2	TX Power High Warning	+5dBm
30-31	2	TX Power Low Warning	+1dBm
32-33	2	RX Power High Alarm	-8dBm
34-35	2	RX Power Low Alarm	-30dBm
36-37	2	RX Power High Warning	-10dBm
38-39	2	RX Power Low Warning	-28dBm
40-55	16	Reserved	
		Calibration C	constants
56-59	4	RX Power Calibration Data4	Single precision floating-point numbers (various
60-63	4	RX Power Calibration Data3	values at each device)
64-67	4	RX Power Calibration Data2	Single precision floating-point numbers (various

Table 2 Memory contents of Diagnostic Monitor Function



68-71	4	RX Power Calibration Data1	values at each device)
72-75	4	RX Power Calibration Data0	
76-77	2	Bias Calibration Data1	01 00 (fixed)
78-79	2	Bias Calibration Data0	00 00 (fixed)
80-81	2	TX Power Calibration Data1	01 00 (fixed)
82-83	2	TX Power Calibration Data0	00 00 (fixed)
84-85	2	Temperature Calibration Data1	01 00 (fixed)
86-87	2	Temperature Calibration Data0	00 00 (fixed)
88-89	2	Vcc Calibration Data1	01 00 (fixed)
90-91	2	Vcc Calibration Data0	00 00 (fixed)
92-94	3	Reserved	00 00 00 (fixed)
95	1	Check Sum	Checksum of bytes 0-94
		Real Time Diagnostic Mo	onitor Interface
96-97	2	Measured Temperature	Yield to a 16-bit A/D value (see Table 2.1)
98-99	2	Measured Vcc	Yield a 16-bit A/D value (see Table 2.1)
100-101	2	Measured Bias	Yield a 16-bit A/D value (see Table 2.1)
100-101 102-103	2 2	Measured Bias Measured TX Power	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1)
100-101 102-103 104-105	2 2 2	Measured Bias Measured TX Power Measured RX Power	Yield a 16-bit A/D value (see Table 2.1)Yield a 16-bit A/D value (see Table 2.1)Yield a 16-bit A/D value (see Table 2.1)
100-101 102-103 104-105 106-109	2 2 2 4	Measured Bias Measured TX Power Measured RX Power Reserved	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1)
100-101 102-103 104-105 106-109 110	2 2 2 4 1	Measured Bias Measured TX Power Measured RX Power Reserved Logic Status	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) See Table 2.2
100-101 102-103 104-105 106-109 110 111	2 2 2 4 1 1	Measured Bias Measured TX Power Measured RX Power Reserved Logic Status AD Conversion Updates	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) See Table 2.2 See Table 2.2
100-101 102-103 104-105 106-109 110 111 112-119	2 2 4 1 1 8	Measured Bias Measured TX Power Measured RX Power Reserved Logic Status AD Conversion Updates Alarm and Warning Flags	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) See Table 2.2 See Table 2.2 See Table 2.3
100-101 102-103 104-105 106-109 110 111 112-119	2 2 4 1 1 8	Measured Bias Measured TX Power Measured RX Power Reserved Logic Status AD Conversion Updates Alarm and Warning Flags Vendor Spec	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) See Table 2.2 See Table 2.2 See Table 2.3 cific
100-101 102-103 104-105 106-109 110 111 112-119 120-127	2 2 4 1 1 8 8	Measured Bias Measured TX Power Measured RX Power Reserved Logic Status AD Conversion Updates Alarm and Warning Flags Vendor Specific	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) See Table 2.2 See Table 2.2 See Table 2.3 cific Don't Access
100-101 102-103 104-105 106-109 110 111 112-119 120-127 128-247	2 2 4 1 1 8 8 8 120	Measured Bias Measured TX Power Measured RX Power Reserved Logic Status AD Conversion Updates Alarm and Warning Flags Vendor Specific User writable EEPROM	Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) Yield a 16-bit A/D value (see Table 2.1) See Table 2.2 See Table 2.2 See Table 2.3 cific Don't Access

The measured values located at bytes 96-105(in the 2 wire address 0xA2) are raw A/D values (16-bit integers) of transceiver temperature, supply voltage, laser bias current, laser optical output power and received power. All the measured values are "Externally Calibrated", and then it is necessary to convert raw A/D values to real world units by the manner as shown in Table 2.1

Table 2.1 Real Time Diagnostic Monitor Values

Byte	e Name	Description
96	Temperature MSB	Internally measured transceiver temperature. Comply with External Calibration of
97	Temperature LSB	SFF-0472.
98	Vcc MSB	Internally measured supply voltage. Comply with External Calibration of SEE 9472
99	Vcc LSB	internally measured supply voltage. Comply with External Calibration of SFF-6472.
100	Laser Bias MSB	Massured Laser bios surrent. Comply with External Calibration of SEE 9472
101	Laser Bias LSB	measured Laser bias current. Compry with External Calibration of SFF-6472.
102	Tx Power MSB	Massured Ty power Comply with External Calibration of SEE 9473
103	Tx Power LSB	measured 1x power. Comply with External Calibration of SFF-6472.
104	Rx Power MSB	Measured Rx power. Comply with External Calibration of SFF-8472.



105 Rx Power LSB

This transceiver implements two optional status bytes, "Logic States" at byte 110(0xA2)" and "A/D Updated" at byte 111(0xA2) as shown in Table 2.2. "A/D Updated" status bits allow the user to verify if an update from the analog-digital conversion has occurred of the measured values, temperature, Vcc, laser bias, Tx power and Rx power. The user writes the byte to 0x00. Once a conversion is completed for a given value, its bit will change to '1'.

Byte	Bit	Name	Description
110	7	Tx Disable State	Optional digital State of the Tx Disable input pin.
110	6	Soft Tx Disable Control	Not supported (set to 0).
110	5	Reserved	Set to 0.
110	4	Rx Rate Select State	Not supported (set to 1).
110	3	Soft Rate Select Control	Not supported (set to 0).
110	2	Tx Fault	Optional digital state of the Tx Fault output pin.
110	1	LOS	Not supported.
110	0	Power on Logic	Bit will be 0 when the analog monitoring is active.
111	7	Temp A/D Valid	Indicates A/D value in Bytes 96/97 is valid.
111	6	Vcc A/D Valid	Indicates A/D value in Bytes 98/99 is valid.
111	5	Laser Bias A/D Valid	Indicates A/D value in Bytes 100/101 is valid.
111	4	Tx Power A/D Valid	Indicates A/D value in Bytes 102/103 is valid.
111	3	Rx Power A/D Valid	Indicates A/D value in Bytes 104/105 is valid.
111	2	Reserved	Set to 0.
111	1	Reserved	Set to 0.
111	0	Reserved	Set to 0.

Table 2.2 Logic Status and AD Conversion Updates

Each of the measured values has a corresponding high alarm, low alarm, high warning and low warning threshold level at location 00-39(0xA2) written as the data format of a corresponding valued shown in Table 2.3. Alarm and warning flags at bytes 112-119(0xA2) are defined as follows.

- (1) Alarm flags indicate conditions likely to result (or have resulted) in link failure and cause for immediate action.
- (2) Warning flags indicate conditions outside the guaranteed operating specification of transceiver but not necessarily causes of immediate link failures.

Table 2.3 Alarm and Warning Flags

Byte	Bit(s)	Name	Description			
112	7	Temperature High Alarm	Set when temperature monitor value exceeds high alarm level.			
112	6	Temperature Low Alarm	Set when temperature monitor value exceeds low alarm level.			
112	5	Vcc High Alarm	Set when Vcc monitor value exceeds high alarm level.			
112	4	Vcc Low Alarm	Set when Vcc monitor value exceeds Low alarm level.			
112	3	Laser Bias High Alarm	Set when laser bias monitor value exceeds high alarm level.			
112	2	Laser Bias Low Alarm	Set when laser bias monitor value exceeds low alarm level.			
112	1	Tx Power High Alarm	Set when Tx power monitor value exceeds high alarm level			
112	0	Tx Power Low Alarm	Set when Tx power monitor value exceeds low alarm level.			
113	7	Rx Power High Alarm	Set when Rx power monitor value exceeds high alarm level			



113	6	Rx Power Low Alarm	Set when Rx power monitor value exceeds low alarm level
113	5-0	Reserved	All bits set to 0.
114	7-0	Reserved	All bits set to 0.
115	7-0	Reserved	All bits set to 0.
116	7	Temperature High warning	Set when temperature monitor value exceeds high warning level.
116	6	Temperature Low warning	Set when temperature monitor value exceeds low warning level.
116	5	Vcc High warning	Set when Vcc monitor value exceeds high warning level.
116	4	Vcc Low warning	Set when Vcc monitor value exceeds Low warning level.
116	3	Laser Bias High warning	Set when laser bias monitor value exceeds high warning level.
116	2	Laser Bias Low warning	Set when laser bias monitor value exceeds low warning level.
116	1	Tx Power High warning	Set when Tx power monitor value exceeds high warning level
116	0	Tx Power Low warning	Set when Tx power monitor value exceeds low warning level.
117	7	Rx Power High warning	Set when Rx power monitor value exceeds high warning level
117	6	Rx Power Low warning	Set when Rx power monitor value exceeds low warning level
117	5-0	Reserved	All bits set to 0.
118	7-0	Reserved	All bits set to 0.
119	7-0	Reserved	All bits set to 0.

Pin Description



Top of Board



Bottom of Board (as viewed thru top of board)

Pin	Name	Function/Description	Engagement order	Notes
1	VeeT	Transmitter Ground	1	
2	TX Fault	Transmitter Fault Indication	3	1
3	TX Disable	Transmitter Disable-Module disables on high or open	3	2



4	MOD-DEF2	Module Definition 2-Two wire serial ID interface	3	3
5	MOD-DEF1	Module Definition 1-Two wire serial ID interface	3	3
6	MOD-DEF0	Module Definition 0-Two wire serial ID interface	3	3
7	Reset	Reset signal input	3	8
8	BPD	Burst Power Detect (active HIGH)	3	4
9	Trigger	Trigger input of burst signal packet received	3	9
10	VeeR	Receiver Ground	1	
11	VeeR	Receiver Ground	1	
12	RD-	Inverted Received Data out	3	5
13	RD+	Received Data out	3	5
14	VeeR	Receiver Ground	1	
15	VccR	Receiver Power supply, +3.3V±5%	2	6
16	VccT	Transmitter Power supply, +3.3 V±5%	2	6
17	VeeT	Transmitter Ground	1	
18	TD+	Transmitter Data In	3	7
19	TD-	Inverted Transmitter Data In	3	7
20	VeeT	Transmitter Ground	1	

Note1: TX Fault is open collector/drain output which should be pulled up externally with a $4.7K - 10K \Omega$ resistor on the host board to supply <VccT+0.3V or VccR+0.3V. When high, this output indicates a laser fault of some kind. Low indicates normal operation. In the low state, the output will be pulled to <0.8V.

Note2: TX Disable input is used to shut down the laser output per the state table below. It is pulled up within the module with a 4.7 ~ 10K resistor.

Low (0 – 0.8V):Transmitter onBetween (0.8V and 2V):UndefinedHigh (2.0 – VccT):Transmitter DisabledOpen :Transmitter Disabled

Note3: Mod-Def 0, 1, 2. These are the module definition pins. They should be pulled up with a 4.7 - 10K resistor on the host board to supply less than VccT+0.3V or VccR+0.3V.

Mod-Def 0 is grounded by the module to indicate that the module is present.

Mod-Def 1 is clock line of two wire serial interface for optional serial ID.

Mod-Def 2 is data line of two wire serial interface for optional serial ID.

Note4: BPD (Burst Power Detect) is pulled up internally with a 10K resistor to VccR. When LOW, this output indicates the received optical power is below the worst case receiver sensitivity (as defined by the standard in use). HIGH indicates normal operation. In the low state, the output will be pulled to <0.8V.

Note5: RD-/+: These are the differential receiver outputs. They are DC coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the user SERDES. The DC coupling is done inside the module and require LVPECL terminal on the host board.

Note6: VccR and VccT are the receiver and transmitter power supplies. They are defined as $3.3V \pm 5\%$ at the SFP connector pin. The in-rush current will typically be no more than 30mA above steady state supply current after 500ns.

Note7: TD-/+: These are the differential transmitter inputs. They are AC coupled differential lines with 100 Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on host board.

Note8: Reset input compliant with LVTTL. It will be asserted HIGH at the end of a burst packet.

Note9: Trigger input compliant with LVTTL. One positive pulse will issue a burst optical power conversion.



Block diagram



Typical application circuit





Package outline

Units in mm



Regulatory Compliance

Feature	Test Method	Performance			
Electrostatic Discharge (ESD)	MIL-STD-883E	Class 1 (, 1 Ek)) - Livrage Derby Marial			
to the Electrical Pins	Method 3015.7	Class T (>T.SKV) – Human Body Model			
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2	Class 2(>4.0kV)			
Electromagnetic Interference	CISPR22 ITE Class B	Compliant with standards			
(EMI)	EN55022 Class B				
	IEC61000 4 2 Class 2	Typically show no measurable effect from a 3V/m			
Immunity		field swept from 80 to 1000MHz applied to the			
	EN55024	transceiver without a chassis enclosure.			
	FDA 21 CFR 1040.10				
	and 1040.11				
Eye Safety	UL	Compliant with Class 1 laser product			
	TUV EN 60825-1				



Ordering information

	Specification							Annlingtion		
Part No.	Package	TX Data Rate	Laser	Optical Power	Detector	RX Data Rate	Sensitivity	Temp	Standard	Code
RTXM167-522	SFP	2.488Gb/s	1490nm DFB	1.5~5dBm	APD	1.244Gb/s	<-28dBm	0~70°C	GPON OLT Class B+	CLASS B+

Note1: Single SC receptacle optical interface compliant

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